Project: CO-packaged Reconfigurable Signal and Intelligence Architecture (CORSAIR): Electronic Warfare (EW)

Problem: The CORSAIR project seeks to provide an EW solution for a multi-chip package with high-speed data converters and in-line accelerators. Today's EW system performance and adaptability are limited by Size, Weight, Power, and Cost (SWaP-C). Power and latency-efficient systems such as ASICs and CPUs are largely static and cannot change functionality dynamically while programmable systems such as Field Programmable Gate Arrays (FPGAs) and Graphical Processing Units (GPUs) don't meet power and latency requirements.

Solution: CORSAIR will develop a fully programmable, RF-enabled dual-use chiplet targeting >20x system-level performance versus incumbent technology in signal processing. Domestically built on Intel's dual-use, 18A-based Configurable Spatial Architecture (CSA), the project will deliver a prototype multi-chip package (MCP) integrating a CSA chiplet with an Intel Agilex 9 direct RF drive device to provide wideband, rapidly reconfigurable RF processing. CSA executes dataflow, an explicitly parallel architectural paradigm in which programs are represented as graphs of computation and data communication. Once configured, CSA computes like a fixed-function pipeline with minimized switching in the chiplet fabric, fundamentally improving silicon and programmability metrics versus currently deployed runtime reconfigurable array architectures (RTRA). The CORSAIR prototype performance and reconfigurability are expected to transform the art of the possible in spectrum sensing. Modeling has shown an average processing gain of 16 dB versus conventional iso-process FPGAs, with 20 dB of gain in estimated EW applications and sub-100 nanosecond switching latency, achieved through a combination of high-performance memory systems, a small program file, and specialized execution and caching techniques enabled by dataflow. This project is expected to mature the CSA components from TRL/MRL 4 to a capability to produce prototypes in a production environment (MRL 6/7).

Project Performers / Role:

- **Lockheed Martin:** Project prime. Hardware and software design support for dual-use Intel 18A co-design focused on processor design, platform/mission SWaP constraints, EW requirements, and operational needs. Application modeling, simulation, and software development. Prototype demonstration and testing.
- **Intel Corporation:** Device design, performance simulation, emulation, fabrication, prototype packaging, testing, and evaluation support.
- **Air Force Research Laboratory / Sensors Directorate:** Performance simulation, emulation, testing, evaluation, and data sets generation.

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